IN THE CLAIMS

Please amend claims 4, 8, 10, 15, 19 and 21 as indicated below.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (original) A device (100) for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said device comprising

at least two ports (102 to 108)) for receiving said at least two data signals,

a port scanning unit (110) for extracting data from the data signals received by said ports, characterized in that said port scanning unit (110) is configured to extract data from ports providing data streams having at least two different input data rates.

Claim 2 (original) The device according to claim 1, further comprising a control logic unit functionally connected to said port scanning unit (110) for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate.

Claim 3 (original) The device according to claim 2, wherein the control logic unit is configured to control said port scanning unit (10) to access a port having a higher input data rate proportionally more often than a port having a lower input data rate.

Claim 4 (currently amended) ~~The device according to claim 1, further comprising~~ A device (100) for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said device comprising

at least two ports (102 to 108)) for receiving said at least two data signals,

a port scanning unit (110) for extracting data from the data signals received by said ports, characterized in that said port scanning unit (110) is configured to extract data from ports providing data streams having at least two different input data rates, and

at least two demultiplexing units for converting said at least two data signals into a parallel data stream of a predetermined width.

Claim 5 (original) The device according to claim 4, further comprising at least two storage units each functionally connected to said port scanning unit (110) and one of said demultiplexing units for temporarily storing data.

Claim 6 (original) The device according to claim 5, wherein the storage unit is formed by a FIFO and said FIFO is configured to operate with a speed corresponding to the input data rate of the connected port.

Claim 7 (original) The device according to claim 2, further comprising a central buffer connected to said port scanning unit (110) into which data from all ports are written.

Claim 8 (currently amended) ~~The device according to claim 7,~~ A device (100) for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said device comprising

at least two ports (102 to 108)) for receiving said at least two data signals,

a port scanning unit (110) for extracting data from the data signals received by said ports, characterized in that said port scanning unit (110) is configured to extract data from ports providing data streams having at least two different input data rates,

a control logic unit functionally connected to said port scanning unit (110) for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate, and

a central buffer connected to said port scanning unit (110) into which data from all ports are written,

wherein the control logic unit is configured to control said port scanning unit (110) to read per access from a port having a higher input data rate proportionally more data than from a port having a lower input data rate and writing the data into said central buffer with a single clock speed.

Claim 9 (original) The device according to claim 7 or 8, further comprising at least two demultiplexing units associated to each port, whereby the resulting data width of a demultiplexing unit is proportionally larger at a port having a higher input data rate.

Claim 10 (currently amended) ~~The device according to claim 7,~~ A device (100) for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said device comprising

at least two ports (102 to 108)) for receiving said at least two data signals,

a port scanning unit (110) for extracting data from the data signals received by said ports, characterized in that said port scanning unit (110) is configured to extract data from ports providing data streams having at least two different input data rates,

a control logic unit functionally connected to said port scanning unit (110) for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate, and

a central buffer connected to said port scanning unit (110) into which data from all ports are written,

wherein the control logic unit is configured to control said port scanning unit (110) to read per access from all ports the same amount of data and writing the data from a port having a higher input data rate proportionally more often into said central buffer than from a port having a lower input data rate.

Claim 11 (original) The device according to claim 10, further comprising a byte alignment unit functionally connected to the central buffer to ensure that only frame byte aligned data are written into said central buffer.

Claim 12 (original) A method for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said method comprising the steps of:

receiving said at least two data signals,

extracting data from the data signals received by said ports, characterized by the step of extracting data from ports providing data streams having at least two different input data rates.

Claim 13 (original) The method according to claim 12, further comprising the step of determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate.

Claim 14 (original) The method according to claim 13, further comprising the step of accessing a port having a higher input data rate proportionally more often than a port having a lower input data rate.

Claim 15 (currently amended) ~~The method according to claim 12, further comprising the step of~~ A method for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said method comprising the steps of:

receiving said at least two data signals,

extracting data from the data signals received by said ports, characterized by extracting data from ports providing data streams having at least two different input data rates,

converting said at least two data signals into a parallel data stream of a predetermined width.

Claim 16 (original) The method according to claim 12, further comprising the step of temporarily storing data.

Claim 17 (original) The method according to claim 16, wherein the step of temporarily storing data is performed according to the FIFO concept with a speed corresponding to the input data rate of the connected port.

Claim 18 (original) The method according to claim 13, further comprising the step of writing data from all ports are written in a central buffer.

Claim 19 (currently amended) ~~The method according to claim 18, further comprising the step of~~ A method for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said method comprising the steps of:

receiving said at least two data signals,

extracting data from the data signals received by said ports, characterized by the step of extracting data from ports providing data streams having at least two different input data rates,

determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate,

writing data from all ports are written in a central buffer, and

reading from a port having a higher input data rate proportionally more data than from a port having a lower input data rate and writing the data into said central buffer with a single clock speed.

Claim 20 (original) The method according to claim 18 or 19, further comprising the step of demultiplexing the incoming data stream of each port, whereby the resulting

data width of a demultiplexing unit is proportionally larger at a port having a higher input data rate.

Claim 21 (currently amended) ~~The method according to claim 18, further comprising the step of~~ A method for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said method comprising the steps of:

receiving said at least two data signals,

extracting data from the data signals received by said ports, characterized by the step of extracting data from ports providing data streams having at least two different input data rates,

determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate,

writing data from all ports are written in a central buffer, and

reading per access from all ports the same amount of data and writing the data from a port having a higher input data rate proportionally more often into said central buffer than from a port having a lower input data rate.

Claim 22 (original) The method according to claim 21, further comprising the step of performing a byte alignment to ensure that only frame byte aligned data are written into said central buffer.

Claim 23 (original) A method comprising the acts of:

(a) receiving, in ports of a network device, frames in which at least two data traffic with different transmission rates are encoded;

(b) reading frames from the ports into a receiving path with a port scanning unit;

(c) examining the frames with a plurality of processing units operatively disposed within the receive path;

(d) as each processing unit, in the plurality of processing units, examines the frames extracting data encoded in particular section of said frame and forwarding remaining portion of the frame to downstream processing units;

(e) repeating step (d) by downstream processing units until the payload section of the frame remains;

(f) receiving the payload section of the frame in a payload handling unit which parses the content into specific data types based upon the encoded data.

Claim 24 (original) The method of claim 23 further including the act of receiving the specific data type in a Utopia level 4 interface which transmits the specific data type to a link layer device or DS.sub.3 mapper device.

Claim 25 (original) The method of claim 23 wherein the extracted data is stored in memory units.

Claim 26 (original) A device comprising:

a data scanning unit that accesses ports of a network device to read data frames in which a payload of at least two data traffic at different rates are encoded;

a plurality of storage elements that store information extracted from the data frames;

a plurality of Receive processing units operatively coupled in series, wherein each one of the plurality of processing units is coupled to selected ones of the storage elements and said each one of the plurality of processing units examining the frame and extracting information from predetermined portion of said frame and forwarding the remaining portion of said frame to downstream processing units; and

a payload handler receiving the payload in said frame and parsing the payload to generate different data types embedded in said payload.

Claim 27 (original) The device of claim 26 further including a plurality of transmit processing units operatively coupled in series and cooperating to generate and

transmit to said ports a frame containing a payload of at least two data traffic at different rates.

Claim 28 (original) The device of claim 27 further including a plurality of memories selectively coupled to selected ones of the plurality of transmit processing units.